Final Project, Part II: Using Keypad Scanner as Input Device for Serial Bit Pattern Detector

Due on May 11th, 11:59 pm

Introduction:

The objectives of Part II of the Final Project are:

- Integrate the keypad scanner with an existing working system (pattern detector)
- logic synthesis
- place and route of the netlist for implementation in an FPGA
- Thorough testing of the design in its RTL and hardware abstractions.

Final Project, Part II Description:

Use the 16-key keypad (completed in Part I) as the bit pattern input device for the serial bit pattern detector and the pattern counter you have designed for Lab 2. The bit pattern detector should be able to detect bit pattern "1001", and display the total number of patterns detected on the two 7-segment display using decade mode (with the maximum value of 99). **A third 7-segment display is used to display what key is being pressed.** Use the keypad to input the serial patterns. Please use the 50 MHz clock for your design.

Deliverables:

User's Guide: A user's manual for your design describing the function of your design, and how to use it. Assume that the user has never read your project assignment sheet. After reading your manual, the user should know how to input the bit pattern (using the keypad), and how to verify if your pattern detector is correct. Design a step by step procedure (with a sample bit pattern) to allow the user to follow and verify the results (expected results after inputting the complete bit pattern should be included). You can modify on top of your Lab 2 user's manual.

(ii) **Design report:** This is the documentation of your entire Final Project (Part I and II). It should describe the design architecture, state diagram, flow chart etc. It should also include the top level block diagram showing how different modules are connected with interfacing signals clearly defined. Include a brief description of each top level module in the design. Each top level signal should be listed in the document with a brief explanation. If handshaking is used between modules, a timing diagram on the interface signals is needed. Design details of the scanner core and the LFSR need to be included. For the LFSR, include detailed calculation of the number of bits needed, the LFSR type chosen and the terminal sequence. Also include the timing diagram for the interface between the LFSR and the scanner core. For the scanner core, include the timing diagram for four sequential scans (see definition in hints). Include state diagram and design details for the scanner core. **To ensure the quality of the document, this report should be developed along with your RTL coding.**

(iii) Synthesizable RTL Verilog code for the Final Project (including all Keypad scanner code and the pattern detector code modified for the final project).

(iv) Board demonstration to the TA. Demonstration is to be done AFTER you have finished and submitted your deliverables to the dropfolder. You need to demonstrate to the TA **by May 13th** during arranged TA lab hours. You are only allowed to use the code downloaded from the dropfolder for demonstration. No new code is allowed!!! All team members have to be present for demonstration. Please bring a hardcopy of your user manual to the TA during the demonstration.

Resources:

Project Hardware Kit – Provided:

1) Altera DE2 board with power supply
2) USB download cable
3) 16-key keypad with 4 row pins and 4 column pins
4) 40-pin ribbon cable

Project Development Toolkit provided:

1) Keypad BFM and sample testbench
2) LFSR Utility

Submission:

All submissions should be deposited in the dropfolder. Make sure that you include at least THREE directories: ModelSim project folder, folder for archive of your QUARTUS II files (.qar file), and the document folder. Please include a README file stating the status of the final project at the time of submission.

Due Date:

This lab is due electronically (via dropfolder) by 11:59 p.m. on May 11th. You have to demonstrate to the TA by May 13th.